

General Purpose NPN Transistor Array

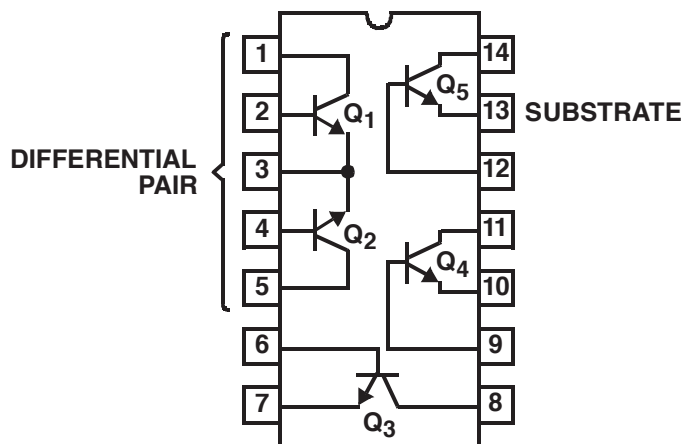
The V3046M consists of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

The transistors of the V3046M are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

Pinout

V3046M (SOIC14)

TOP VIEW



Features

- Two Matched Transistors
 - V_{BE} Match..... ± 5 mV
 - I_{IO} Match.....2 μ A (Max)
- Low Noise Figure.....3.2 dB (Typ) at 1 kHz
- 5 General Purpose Monolithic Transistors
- Operation From DC to 120 MHz
- Wide Operating Current Range
- Full Military Temperature Range

Applications

- Three Isolated Transistors and One Differentially Connected Transistor Pair for Low Power Applications at Frequencies from DC Through the VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers

Absolute Maximum Ratings

Collector-to-Emitter Voltage (V_{CE0})	15 V
Collector-to-Base Voltage (V_{CBO})	20 V
Collector-to-Substrate Voltage (V_{CIO} , Note 1)	20 V
Emitter-to-Base Voltage (V_{EBO})	5 V
Collector Current (I_C)	50 mA

Operating Conditions

Temperature Change -55 °C to 125 °C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package	220	N/A
Maximum Power Dissipation (Any One Transistor)	300 mW	
Maximum Junction Temperature (Plastic Package)	150 °C	
Maximum Storage Temperature Range	-65 °C to 150 °C	
Maximum Lead Temperature (Soldering 10s)	300 °C (SOIC - Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the V3046M is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25$ °C, characteristics apply for each transistor in V3046M as specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC CHARACTERISTICS						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10 \mu A, I_E = 0$	20	60	—	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1 mA, I_B = 0$	15	24	—	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10 \mu A, I_{CI} = 0$	20	60	—	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10 \mu A, I_C = 0$	5	7	—	V
Collector Cutoff Current (Figure 1)	I_{CBO}	$V_{CB} = 10 V, I_E = 0$	—	0.002	4.0	nA
Collector Cutoff Current (Figure 2)	I_{CEO}	$V_{CE} = 10 V, I_B = 0$	—	See Fig. 2	0.5	μA
Forward Current Transfer Ratio (Static Beta) (Note 3) (Figure 3)	h_{fe}	$V_{CE} = 3 V$	$I_C = 10 mA$	—	100	—
			$I_C = 1 mA$	40	100	—
			$I_C = 10 \mu A$	—	54	—
Input Offset Current for Matched Pair Q1 and Q2. $ I_{O1} - I_{O2} $ (Note 3) (Figure 4)		$V_{CE} = 3 V, I_C = 1 mA$	—	0.3	2	μA
Base-to-Emitter Voltage (Note 3) (Figure 5)	V_{BE}	$V_{CE} = 3 V$	$I_E = 1 mA$	—	0.715	V
			$I_E = 10 mA$	—	0.800	V
Magnitude of Input Offset Voltage for Differential Pair $ V_{BE1} - V_{BE2} $ (Note 3) (Figures 5, 7)		$V_{CE} = 3 V, I_C = 1 mA$	—	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors $ V_{BE3} - V_{BE4} , V_{BE4} - V_{BE5} , V_{BE5} - V_{BE3} $ (Note 3) (Figures 5, 7)		$V_{CE} = 3 V, I_C = 1 mA$	—	0.45	5	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	—	-1.9	—	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1\text{ mA}, I_C = 10\text{ mA}$	—	0.23	—	V
Temperature Coefficient: Magnitude of Input Offset Voltage (Figure 7)	$\frac{ \Delta V_{IO} }{\Delta T}$	$V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	—	1.1	—	μA/°C

DYNAMIC CHARACTERISTICS

Low Frequency Noise Figure (Figure 9)	NF	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 100\text{ μA}, \text{Source Resistance} = 1\text{ k}\Omega$	—	3.25	—	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics						
Forward Current Transfer Ratio (Figure 11)	h_{FE}	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	—	110	—	—
Short Circuit Input Impedance (Figure 11)	h_{IE}	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	—	3.5	—	kΩ
Open Circuit Output Impedance (Figure 11)	h_{OE}	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	—	15.6	—	μS
Open Circuit Reverse Voltage Transfer Ratio (Figure 11)	h_{RE}	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	—	1.8×10^{-4}	—	—
Admittance Characteristics						
Forward Transfer Admittance (Figure 12)	Y_{FE}	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	—	$31 - j1.5$	—	—
Input Admittance (Figure 13)	Y_{IE}	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	—	$0.3 + j0.04$	—	—
Output Admittance (Figure 14)	Y_{OE}	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	—	$0.001 + j0.03$	—	—
Reverse Transfer Admittance (Figure 15)	Y_{RE}	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	—	See Fig. 14	—	—
Gain Bandwidth Product (Figure 16)	f_T	$V_{CE} = 3\text{ V}, I_C = 3\text{ mA}$	300	550	—	MHz
Emitter-to-Base Capacitance	C_{EB}	$V_{EB} = 3\text{ V}, I_E = 0$	—	0.6	—	pF
Collector-to-Base Capacitance	C_{CB}	$V_{CB} = 3\text{ V}, I_C = 0$	—	0.58	—	pF
Collector-to-Substrate Capacitance	C_{CI}	$V_{CS} = 3\text{ V}, I_C = 0$	—	2.8	—	pF

NOTE:

- Actual forcing current is via the emitter for this test.

Typical Performance Curves

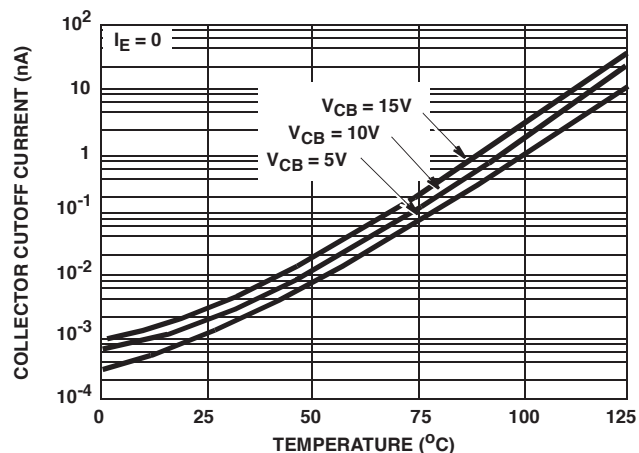


FIGURE 1. TYPICAL COLLECTOR-TO-BASE CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

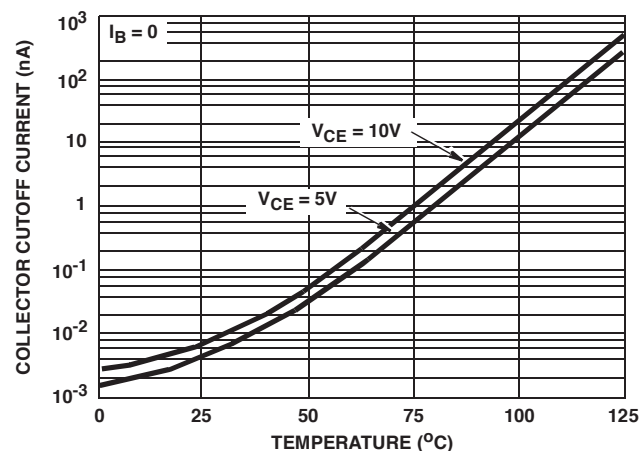


FIGURE 2. TYPICAL COLLECTOR-TO-EMITTER CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

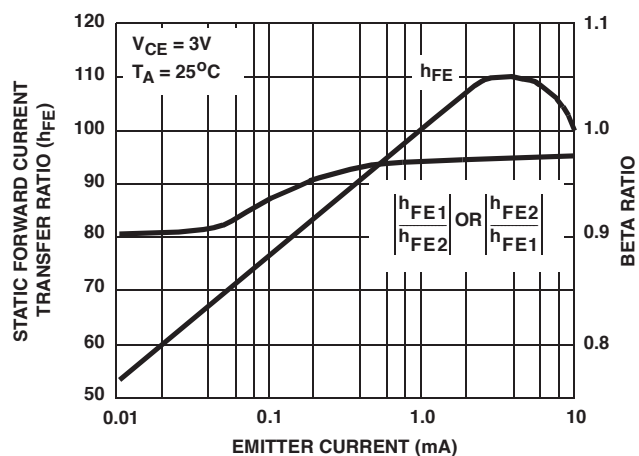


FIGURE 3. TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO AND BETA RATIO FOR Q_1 AND Q_2 vs EMITTER CURRENT

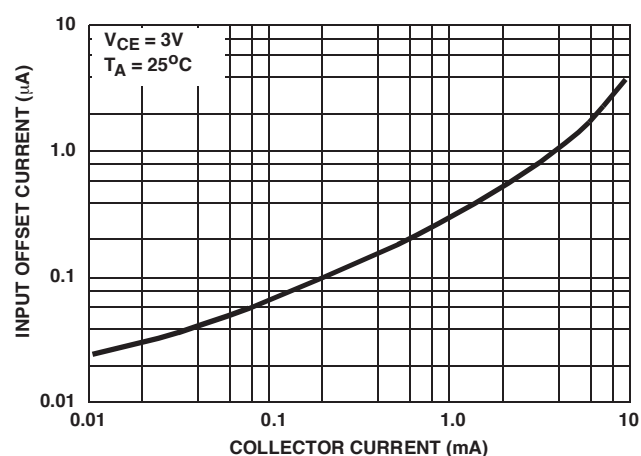


FIGURE 4. TYPICAL INPUT OFFSET CURRENT FOR MATCHED TRANSISTOR PAIR Q_1Q_2 vs COLLECTOR CURRENT

Typical Performance Curves

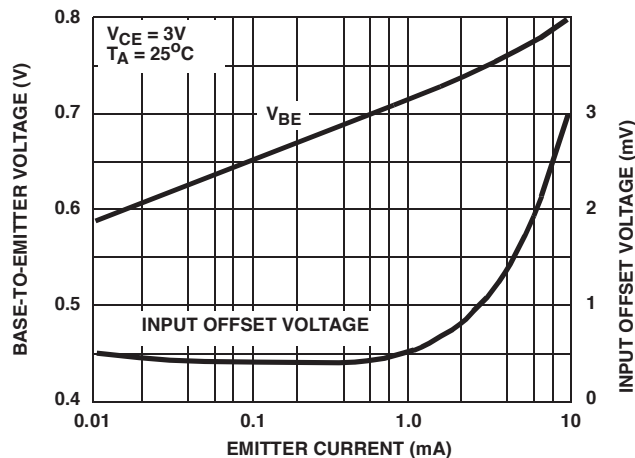


FIGURE 5. TYPICAL STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTICS AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS vs EMITTER CURRENT

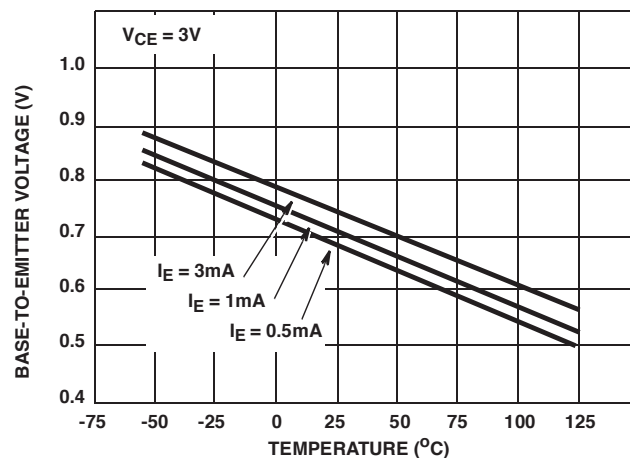


FIGURE 6. TYPICAL BASE-TO-EMITTER VOLTAGE CHARACTERISTIC vs TEMPERATURE FOR EACH TRANSISTOR

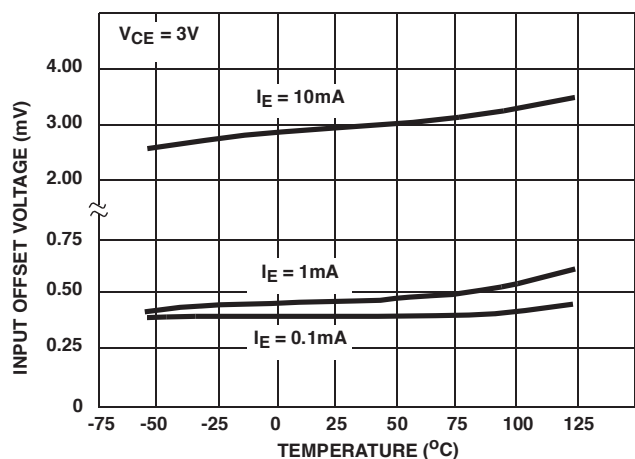


FIGURE 7. TYPICAL INPUT OFFSET VOLTAGE CHARACTERISTICS FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS vs TEMPERATURE

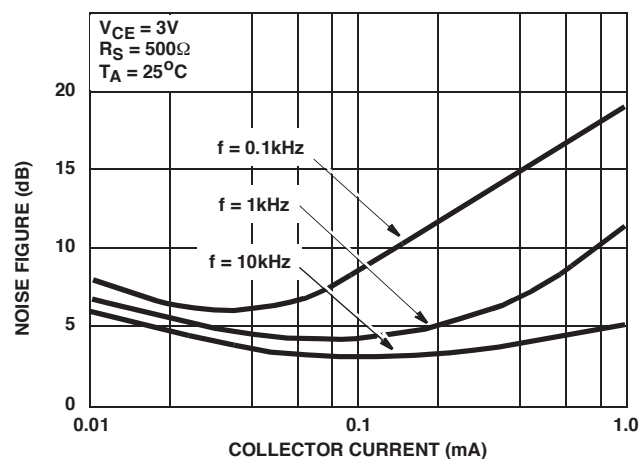


FIGURE 8. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

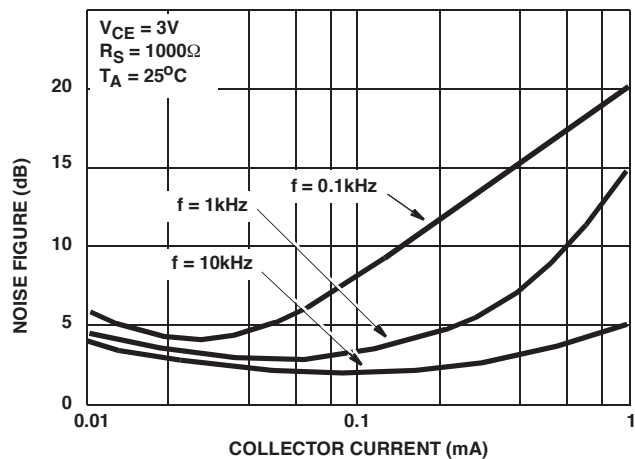


FIGURE 9. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

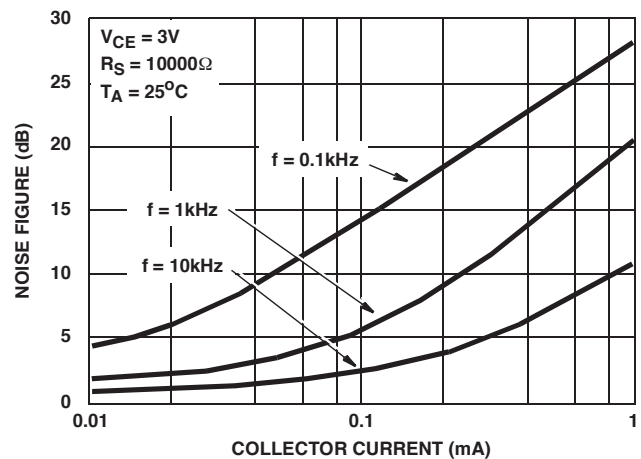


FIGURE 10. TYPICAL NOISE FIGURE vs COLLECTOR CURRENT

Typical Performance Curves

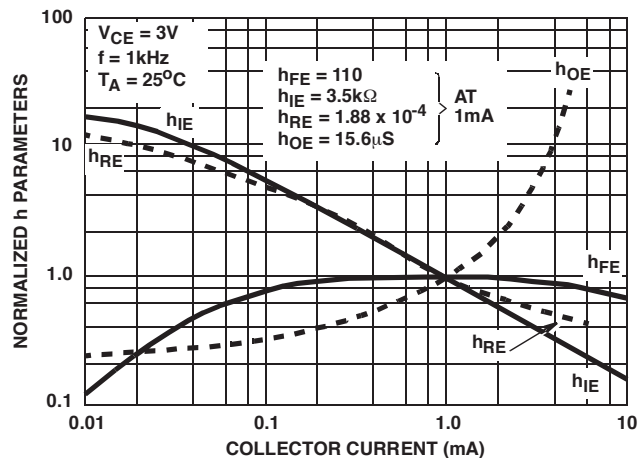


FIGURE 11. TYPICAL NORMALIZED FORWARD CURRENT TRANSFER RATIO, SHORT CIRCUIT INPUT IMPEDANCE, OPEN CIRCUIT OUTPUT IMPEDANCE, AND OPEN CIRCUIT REVERSE VOLTAGE TRANSFER RATIO vs COLLECTOR CURRENT

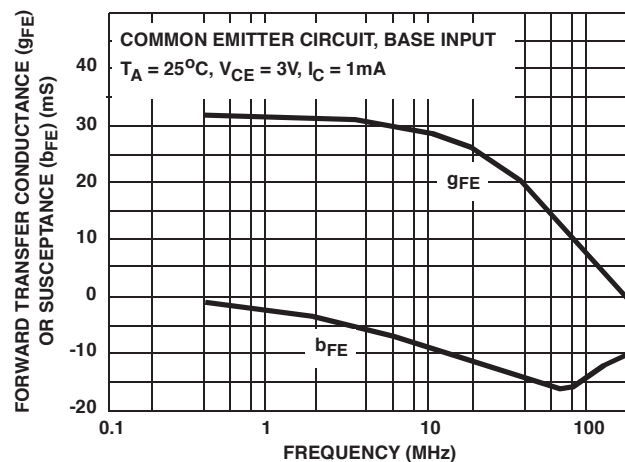


FIGURE 12. TYPICAL FORWARD TRANSFER ADMITTANCE vs FREQUENCY

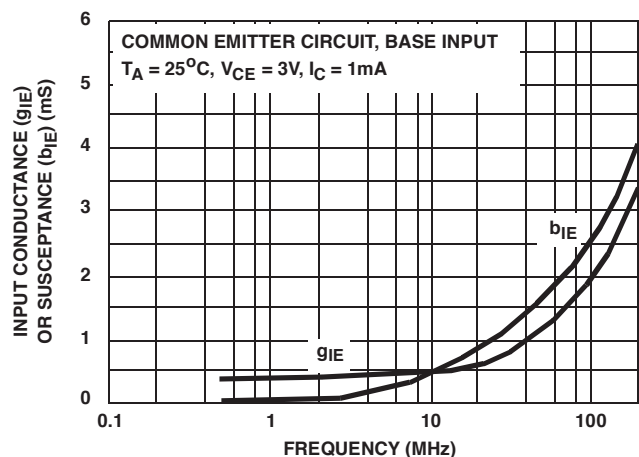


FIGURE 13. TYPICAL INPUT ADMITTANCE vs FREQUENCY

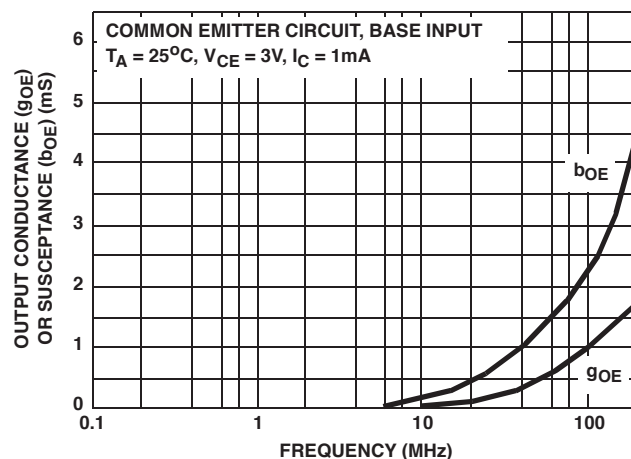


FIGURE 14. TYPICAL OUTPUT ADMITTANCE vs FREQUENCY

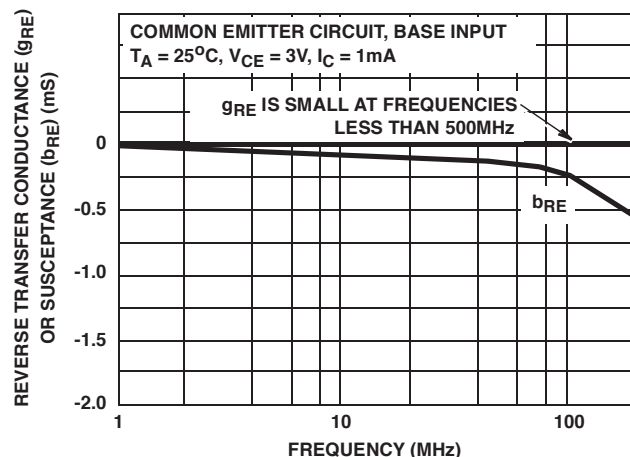


FIGURE 15. TYPICAL REVERSE TRANSFER ADMITTANCE vs FREQUENCY

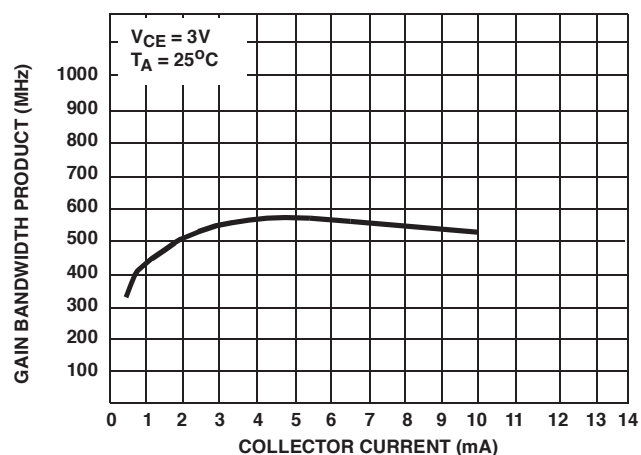
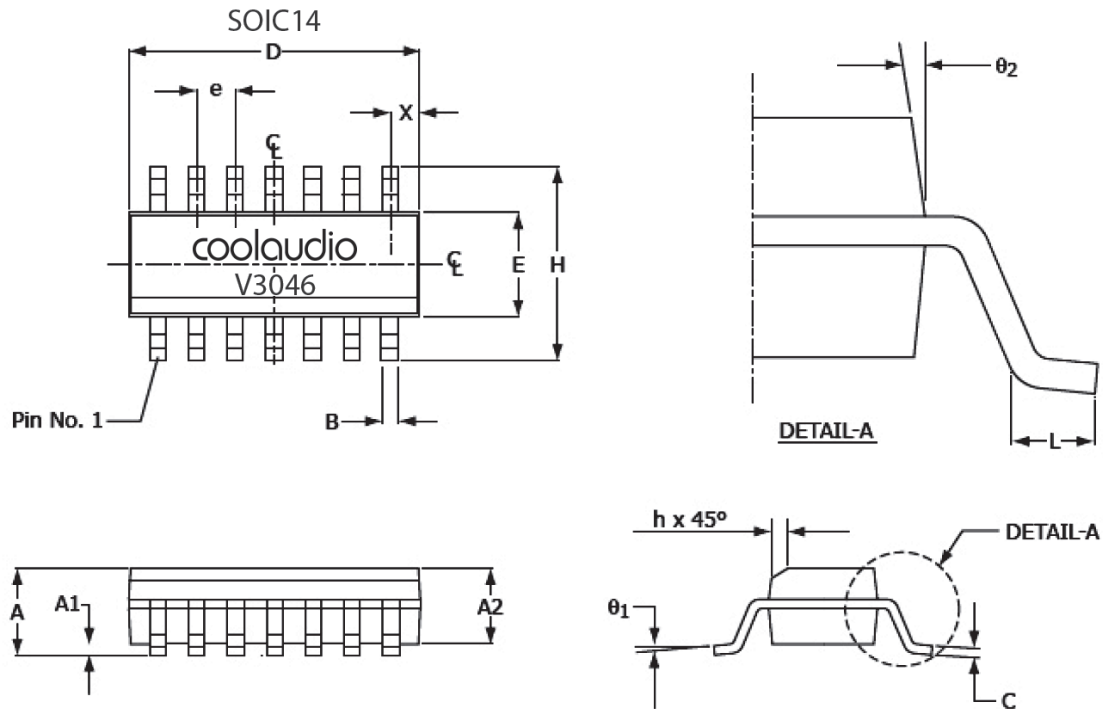


FIGURE 16. TYPICAL GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT



NOTES:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1 mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905 mm from the lead tip.