2048-Stage Low Voltage Operation Low Noise BBD

V3208D/V3208SD

General description

The V3208D/V3208SD is a 2048-stage low voltage operation (VDD = 5V) BBD that provides a signal delay of up to 102.4ms at clock frequency 10KHz and is suitable for use as reverberation effect of audio equipments such as portable stereo and radio cassette recorders which need low voltage and long delay time since S/N is 71dB in spite of many stages.

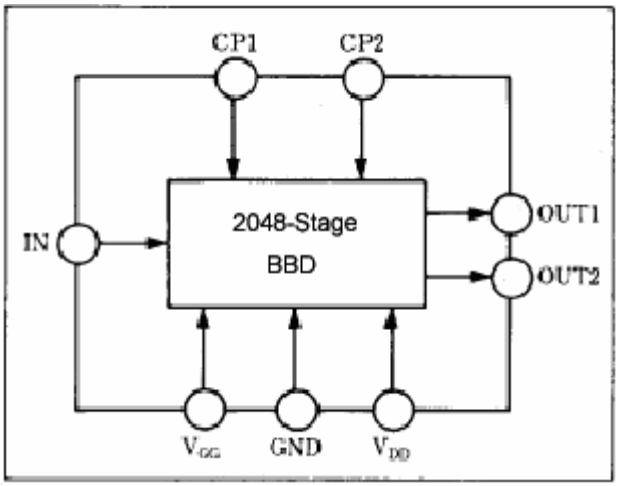
Features

- Variable delay of audio signals: 10.24ms ~ 102.4ms.
- Wide power supply voltage: 4 ~ 10V.
- No insertion noise: Li = 0dB typ.
- Wide dynamic range: S/N = 71dB.
- N Channel silicon gate process.
- DIP8（-DIP8）for V3208D/Special 8-Lead Dual-In-Line plastic Package（-SDIP8）for V3208SD.

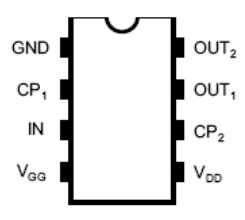
Applications

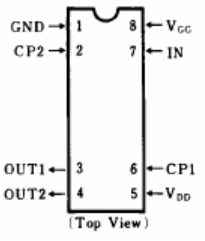
- Reverberation and echo effects of audio equipment such as radio cassette recorder, car radio, portable radio, portable stereo, echo microphone and pre-taped musical accompaniment (Karaoke), etc.
- Sound effect of electronic musical instrument.
- Variable or fixed delay of analog signals.
- Telephone time compression and delay line for voice communication system.

Block Diagram



Pin Configuration

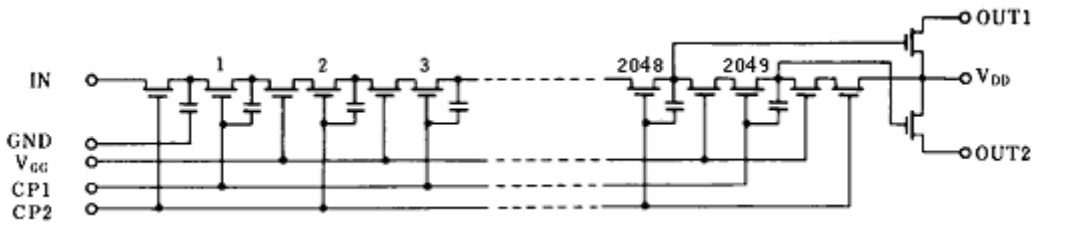




V3208D **V3208SD**

Symbol	Type	Description
GND	P	Ground
CP2	I	The second clock input
OUT1	O	Signal output, delayed 4096 times
OUT2	O	Signal output, delayed 4097 times
V_{DD}	P	Power
CP1	I	The first clock input
IN	I	Analog signal input
V_{GG}	I	Bias voltage input ($^{14}/_{15}V_{DD}$)

Circuit Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD} , V_{GG}	+5, $^{14}/_{15}V_{DD}$	V
Signal Delay Time	t_D	10.24 ~ 102.4	ms
Total Harmonic Distortion	THD	2.5	%
Signal to Noise Ratio	S/N	71	dB

Absolute Maximum Ratings (Ta = 25℃)

Item	Symbol	Rating	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_i	-0.3 ~ +11	V
Output Voltage	V_O	-0.3 ~ +11	V
Operation Ambient Temp.	T_{opr}	-20 ~ +60	℃
Storage Temp.	T_{stg}	-55 ~ +125	℃

Operating Condition (Ta = 25℃)

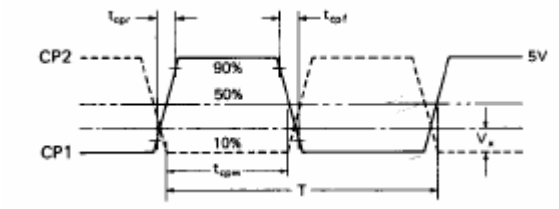
Item	Symbol	Condition	Min.	Typ.	Max	Unit
Drain Supply Voltage	V_{DD}		+4	+5	+10	V
Gate Supply Voltage	V_{GG}			$^{14}/_{15}\ V_{DD}$		V
Clock Voltage High	V_{CPH}			V_{DD}		V
Clock Voltage Low	V_{CPL}		0		+0.5	V
Clock frequency	f_{CP}		10		100	kHz
Clock Pulse Width *1	t_{CPW}				0.5T*2	
Clock Rise Time *1	t_{CPr}				500	ns
Clock fall Time *1	t_{CPf}				500	ns
Clock Input Cap.	C_{CP}				2800	pF
Clock Cross Point	V_X		0		$0.3V_{CPH}$	V

■ Electrical Characteristics

(Ta = 25℃, $V_{DD} = V_{CPH} = 5V$, $V_{CPL} = 0V$, $V_{GG} = {}^{14}/_{15}\ V_{DD}$, R_L=100kΩ)

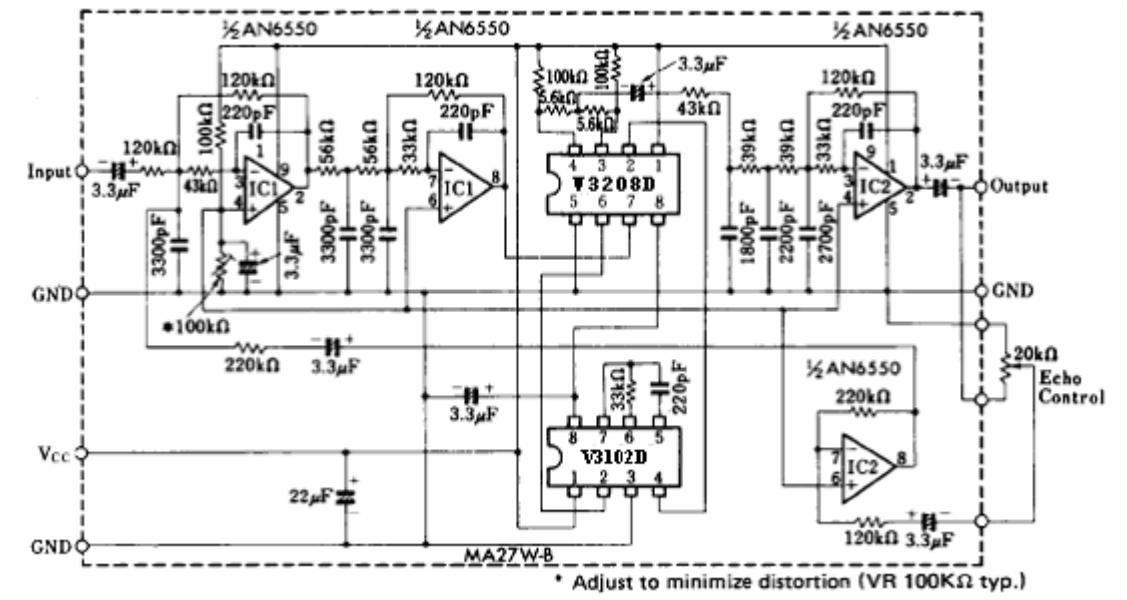
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay time	t_O		10.24		102.4	ms
Input Signal Freq.	f_i	f_{CP} = 40kHz, Output Attenuation ≤ 3dB	10			kHz
Input Signal Swing	V_i	THD = 2.5%		0.36		V_{rms}
Insertion Loss	L_i	f_{CP} = 40kHz, f_i = 1kHz	-4	0	4	dB
Total Harm. Dist.	THD	f_{CP} = 40kHz, f_i = 1kHz, V_i = 0.25 V_{rms}		0.8	2.5	%
Output Noise Voltage	V_{ON}	t_{CP} = 100 kHz,			0.25	mV_{rms}
Signal to Noise Ratio	S/N	Weighted by “A” curve		71		dB

*1 Clock Pulse Waveform

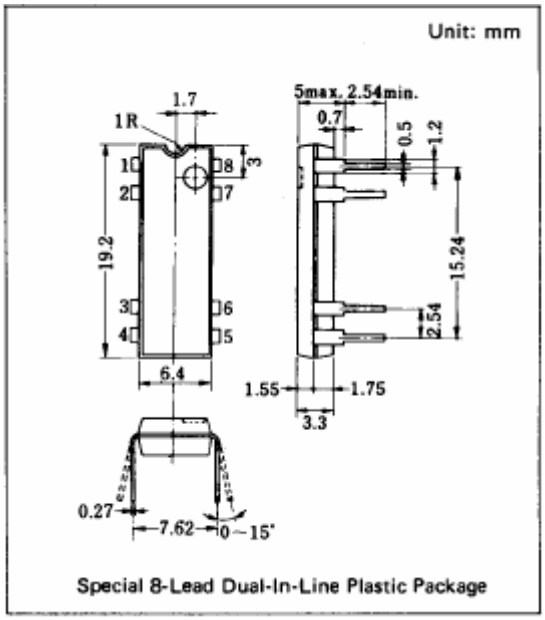


*2 $T = 1/f_{CP}$ (Clock Period)

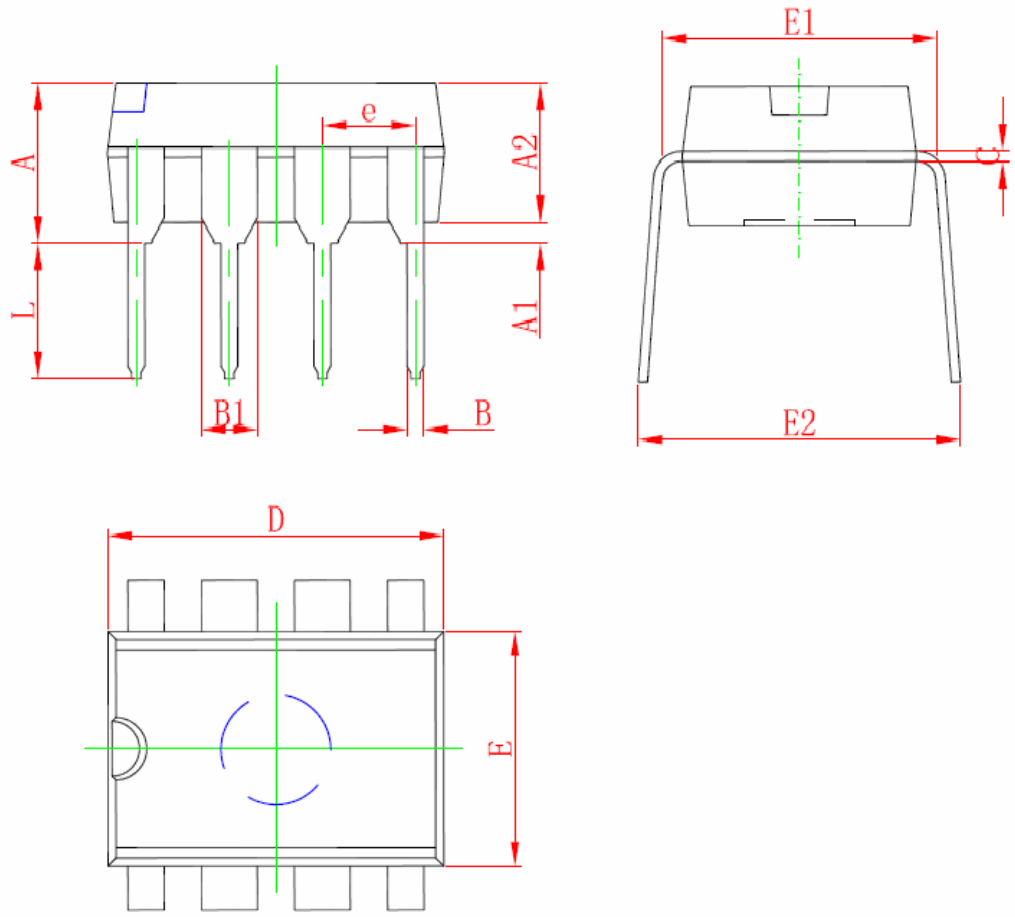
Application Circuit



Mechanical Specification



DIP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354