

General description

The V3205SD is a 4096-stage low voltage operation ($V_{DD} = 5V$) BBD that provides a signal delay of up to 204.8ms at clock frequency 10KHz and is suitable for use as reverberation effect of audio equipments such as portable stereo and radio cassette recorders which need low voltage and long delay time since S/N is 60dB in spite of many stages.

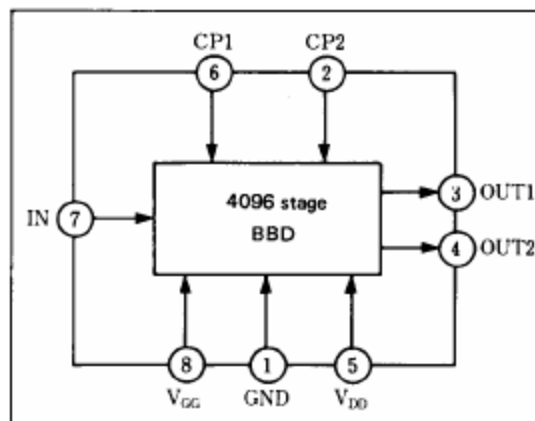
Features

- Variable delay of audio signals: 20.48ms ~ 204.8ms.
- Wide power supply voltage: 4 ~ 8V.
- No insertion noise: $L_i = 0dB$ typ.
- Wide dynamic range: $S/N = 60dB$.
- N Channel silicon gate process.
- Special 8-Lead Dual-In-Line plastic Package.

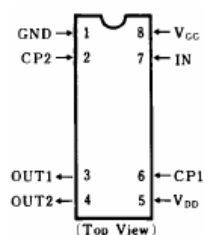
Applications

- Reverberation and echo effects of audio equipment such as radio cassette recorder, car radio, portable radio, portable stereo, echo microphone and pre-taped musical accompaniment (Karaoke), etc.
- Sound effect of electronic musical instrument.
- Variable or fixed delay of analog signals.
- Telephone time compression and delay line for voice communication system.

Block Diagram

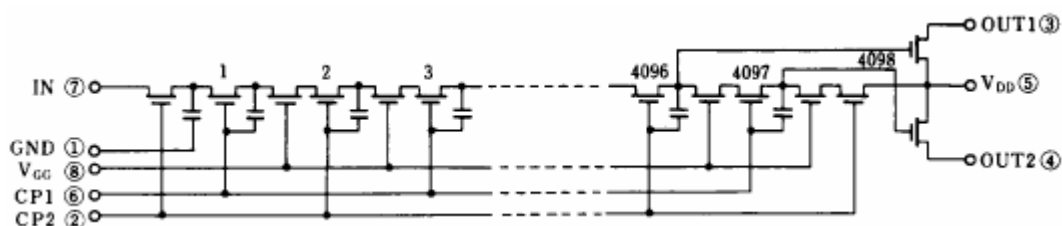


Pin Configuration



No.	Symbol	Type	Description
1	GND	P	Ground
2	CP2	I	The second clock input
3	OUT1	O	Signal output, delayed 4096 times
4	OUT2	O	Signal output, delayed 4097 times
5	V _{DD}	P	Power
6	CP1	I	The first clock input
7	IN	I	Analog signal input
8	V _{GG}	I	Bias voltage input ($^{14}/_{15}V_{DD}$)

Circuit Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V _{DD} , V _{GG}	+5, $^{14}/_{15}V_{DD}$	V
Signal Delay Time	t _D	20.48 ~ 204.8	ms
Total Harmonic Distortion	THD	0.8	%
Signal to Noise Ratio	S/N	60	dB

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Terminal Voltage	V _{DD} , V _{GG} , V _{CP} , V _i	-0.3 ~ +11	V
Output Voltage	V _O	-0.3 ~ +11	V
Operation Ambient Temp.	T _{opr}	-20 ~ +60	°C
Storage Temp.	T _{stg}	-55 ~ +125	°C

Operating Condition (Ta = 25°C)

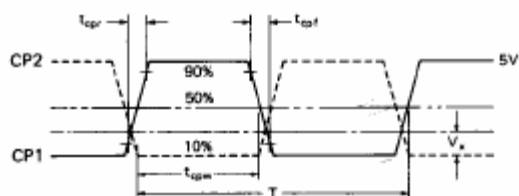
Item	Symbol	Condition	Min.	Typ.	Max	Unit
Drain Supply Voltage	V _{DD}		+4	+5	+8	V
Gate Supply Voltage	V _{GG}			¹⁴ / ₁₅ V _{DD}		V
Clock Voltage High	V _{CPH}			V _{DD}		V
Clock Voltage Low	V _{CPL}		0		+0.5	V
Clock frequency	f _{CP}		10		100	kHz
Clock Pulse Width * ¹	t _{CPW}				0.5T* ²	
Clock Rise Time *1	t _{CPr}				500	ns
Clock fall Time *1	t _{CPf}				500	ns
Clock Input Capatence	C _{CP}				2800	pF
Clock Cross Point	V _X		0		0.3V _{CPH}	V

Electrical Characteristics

(Ta = 25°C, V_{DD} = V_{CPH} = 5V, V_{CPL} = 0V, V_{GG} = 14/15 V_{DD}, RL=100kΩ)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay time	t _O		20.48		204.8	ms
Input Signal Freq.	f _i	f _{CP} = 40kHz, Output Attenuation ≤ 3dB	6			kHz
Input Signal Swing	V _i	THD = 2.5%	0.36			V _{rms}
Insertion Loss	L _i	f _{CP} = 40kHz, f _i = 1kHz	-4	0	4	dB
Total Harm. Dist.	THD	f _{CP} = 40kHz, f _i = 1kHz, V _i = 0.25 V _{rms}		0.8	2.5	%
Output Noise Voltage	V _{ON}	t _{CP} = 100 kHz,			0.35	mV _{rms}
Signal to Noise Ratio	S/N	Weighted by "A" curve		60		dB

*¹ Clock Pulse Waveform



*² T = 1/f_{CP} (Clock Period)

