CLOCK AND SYNCHRONIZATION IN SYSTEM 6000

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Introduction

This document will discuss the clock, synchronization and interface design of TC System 6000 and deal with several of the factors that must be considered when using a digital studio. We will go through different aspects in this area e.g.

- What is jitter, what causes it and how is it removed on System 6000.
- Measurements comparing a conventional clock design to that of System 6000.
- Synchronization in digital audio studios in general.

The article is addressed to the users of System 6000 and other high-end digital studio equipment. It is meant to be a guide to an optimized digital studio setup. It is our experience that many of the problems in a digital setup can be solved by knowledge alone, so hopefully the document will help to answer some of the questions and to clear some of the typical misunderstandings relating to timing and clock generation.

Quality of AD and DA conversion

When designing System 6000 and its ADA24/94 analog conversion card we looked carefully at a lot of parameters in order to reach the highest possible overall performance…

- Frequency response
- Distortion
- Noise
- Crosstalk
- Common mode signals
- Alias filtering
- Jitter
- Analog domain pre/post scaling of converters
- Analog outputs optimized for balanced as well as unbalanced operation

After AD conversion, the analog signal is represented only as a level and timing component. Lack of precision in either area is detrimental to the process, so talking about a converter being "20" or even "24" bit provides very little information if the timing source is not equally well quantified.

What is jitter?

Jitter is the variation in time of a clock signal from the ideal. The amount and rate of the variation are the important parameters. Research made through the last years suggests that variations faster than 500 Hz are the most audible [1]. If you are not familiar with the jitter terminology it is important to notice that the sampling frequency (Fs) could be 48.000 kHz (or maybe 256 times Fs equals 12.288 MHz) and that it is the variation of this clock that has to be faster than 500Hz.

Jitter performance is measured in seconds and a typical value could be in the area of 100 ps peak to 50 ns peak (jitter is also often measured in peak to peak or RMS). The typical jitter frequency spectrum tends to be low frequency weighted.

Clock wander (clock frequency change over long time) is also a kind of jitter but is so slow that it probably hasn't got a direct influence on the sound. Clock wander is typically due to temperature change and aging of the clock crystals in a device.

Sampling jitter.
Jitter only affects the sound quality when occurring in relation with converters (Digital to Analog Converter DAC, ADC or an Asynchronous Sample Rate Converter ASRC).

If the clock controlling an analog to digital conversion is subject to significant jitter, the signal gets converted at unknown points in time. Then, when playing back the digital signal even by using a rock steady clock, the signal is no longer identical to the first analog signal. You could say that the time variation on the first clock has been modulated onto the signal and therefore the signal is now distorted.

Sampling jitter is a potential problem every time the signal changes domain like in a DAC, ADC or an ASRC and as a rule of thumb the internal clock of a digital audio device is better jitter wise than when the device is clocked from a digital input.

This is why quality concious mastering studios put their ADC in internal clock mode when feeding in analog material, but switch to DA clocking when all material is loaded. The converter performing the most critical task (capturing or monitoring) is assigned the master clock role.

System 6000 is one of the first pro audio devices seriously tackling the dilemma of which clock to use as master - AD or DA. First of all, AD and DA share the same very local, high quality clock. Secondly, even if an external clock is used, its jitter is so attenuated, that it has no effect on the conversion.

Interface jitter.
Interface jitter does not directly influence the sound. In extreme cases, however, interface jitter can be so severe that the transmission breaks down. At his point, of course, audio quality will indeed be affected.

Interface jitter is the variation in time of the electrical signal (carrying the digitized audio) being transferred between two devices. The main issue in order for the interface to work is that the receiving device is able to follow the timing variations well enough to receive the correct data.

Often, a device receiving a digital signal is slave to the incoming signal. This means that the device extracts the clock from the incoming digital signal in order to be

synchronized to the transmitting device. In conventional circuit designs the extracted clock is typically used directly for the converters. This means that the jitter on the digital interface is fed nearly unaltered to the converters and therefore manifests as sampling jitter.

Causes of Jitter

There are several ways that jitter find it's way into a digital studio setup.

Noise induced on cables

A digital receiver typically detects a rising or a falling edge on a digital signal at approx. halfway level. Due to finite rise/fall times on the signal, noise then can disturb the detection so the receiver detects the egdes imprecisely. Therefore, both noise and other interference imposed on the signal line and the slope of the signal edge has influence on the precision of the receiver. Some digital formats are unbalanced (coaxial-S/PDIF) and others are balanced (AES/EBU). The balanced signals are more immune to induced noise due to the noise being treated as a common mode signal, which is suppressed to some extend in the receiving device.

Data jitter (or program jitter)

Data jitter is caused by high frequency loss in cables and the nature of some digital formats (e.g. AES/EBU and S/PDIF). Because the electrical data patterns are irregular and changes all the time, a specific edge in the signal can arrive at different times depending on the data pattern prior to the edge. If there weren't any high frequency loss in the cable this wouldn't be the case.

By using cables with incorrect impedance there will be a non-ideal transmission line that potentially contributes to the sloped edges and high frequency loss, and therefore indirectly generates jitter. In this respect, unbalanced formats (like S/PDIF) is often superior to its balanced counterparts.

Optical formats

Some digital formats are optical (Toslink-S/PDIF and ADAT) and they have a reputation of being bad formats jitter wise. One of the reasons for this is that the most common circuits used for converting between electrical and optical signal are better at making a rising than a falling edge. This causes asymmetries in the transferred digital signal, which also contribute to data jitter.

Internal design

Every oscillator or PLL (phase locked loop) will be uncertain about the time to some extent. (A PLL is typically used to multiply frequencies or to filter a clock signal in order to reduce jitter - jitter rejection).
This kind of basic incertainty is called intrinsic jitter and for cheap designs it can be quite severe (there are examples of up to 300ns peak where the limit for the AES format is 4 ns peak @ 48 kHz Fs, BW: 700 to 100 kHz [3]).
Devices that feature jitter rejection will typically be well designed regarding intrinsic jitter as well.

Jitter accumulation

Jitter accumulation can happen in a chain of devices due to intrinsic jitter PLUS jitter gain (see The clock design on System 6000) in devices PLUS cable introduced jitter. Every device and cable will add a bit of jitter and in the end the jitter amount can get disturbing. There are ways to overcome this potential problem (see Synchronization).

How to detect jitter in the system

How to detect sampling jitter

The higher rise/fall time of the program signal the more sensitive it is to sample clock jitter and therefore one of the best ways to analyze a converter performance jitter wise is to apply a full-scale high frequency sine to the converter. The sample clock jitter will then be modulated onto the audio signal and it is now possible to measure the jitter frequency spectrum by performing an FFT on the converted audio signal.

In Figure 1 the DAC has been converting a 12 kHz sine. The two curves illustrate the difference with and without 5 kHz 3.5ns RMS jitter being applied on the digital interface. In this example the device has no rejection of the jitter appearing on the digital interface so it is nearly directly transferred to the converter where it is modulated into the audio signal. A conventional design like this is discussed in more details later.

The two jitter spikes are at the frequencies 12 kHz +/- 5kHz and the level approx. -80 dB corresponds to the 5kHz 3.5ns RMS jitter being applied. Sampling jitter (for jitter frequencies below Fs/2) will appear symmetrically around the sine being converted. Jitter frequencies above Fs/2 will be modulated into the audio signal in a more complex way. Another thing to notice on Figure 1 is that on the curve with 5kHz jitter there is also a tendency of some low frequency < 2 kHz (note 12 kHz +/- 2 kHz) noise jitter. This might be due to noise in the circuit generating the 5 kHz jitter.
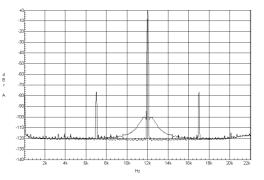

Figure 1 FFT on a DAC. Measurement made on Audio Precision System 2 Cascade using a 2k point FFT with 256 times average, and equiripple window. Two curves: Upper with a 12kHz spike and two 12kHz +/- 5kHz spikes. Lower only with a 12kHz spike.

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How to detect interface jitter.
The typical way to investigate interface jitter is by measuring the clock variations directly on the digital signal. There are devices made specifically for interface testing. The way they usually work is by applying a PLL circuit like the ones used for jitter rejection (see The clock design on System 6000) and then measure the amount that has been stopped by the PLL.

This circuit will act like a low pas filter towards the jitter variations and therefore it is the high frequencies that are stopped by the PLL. This way you will measure the jitter noise with a band limited filter that typically will have settings like 50 to 100 kHz, 700 to 100 kHz and 1200 to 100kHz.

By applying different filters and therefore getting different results you will have an idea of what jitter amount your system is operating at and what jitter frequencies that might be the potential problem.

Examples of interface jitter amounts
A test setup was made with 4 different devices connected using AES/EBU. Short impedance matched cables were used so there was only an insignificant amount of jitter coming from this potential source.

Figure 2. Test setup for interface jitter measurement.

Devices 1 to 3 are conventional designs with no jitter rejection below 10 kHz.
Device 4 is System 6000 (with jitter rejection).

Band width	After device 1	After device 2	After device 3	After device 4
50 to 100 kHz	1.0 ns peak	2.2 ns peak	2.5 ns peak	1.1 ns peak
700 to 100 kHz	0.9 ns peak	1.6 ns peak	1.9 ns peak	0.9 ns peak
1200 to 100 kHz	0.9 ns peak	1.5 ns peak	1.7 ns peak	0.9 ns peak

Table 1 Interface jitter measurements.

In Table 1 the results from the interface jitter measurements are shown. After device 1 the results reflect only intrinsic jitter of this machine. Notice the slight increase at 50Hz, which is common. After device 2 the jitter amount has increased which in this case was due to intrinsic jitter in device 2. The same thing was the case after device 3. After System 6000 (device 4) jitter level has dropped due to the jitter rejection in the system.

There is still an increased level at 50Hz where the System 6000 jitter rejection filter has it's corner frequency and this is why the jitter at 50Hz isn't as reduced as the level above 50Hz.
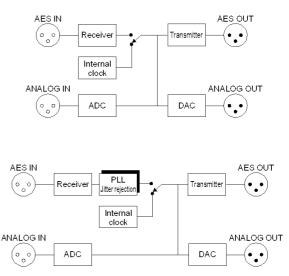
The clock design on System 6000

Figure 3 Clock circuit in a conventional design and in System 6000

Jitter rejection
The secret is the PLL that is used to remove jitter that might appear on the digital input and in a conventional design is transferred nearly directly to the converters. The PLL acts as a low pass filter and will reduce jitter noise of higher frequencies than the corner frequency of the filter. On System 6000 the corner frequency is as low as 50 Hz and at 1.4 kHz the noise will be reduced by at least 100 dB. Figure 4 shows -69dB at 500 Hz, which corresponds to filter suggestions, made from research in the last year's [1].
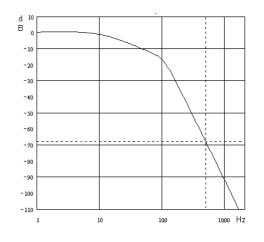
Figure 4 Jitter rejection filter (4'Th order filter)

It is very difficult to design a low pass filter with a steep slope without gain in the pass band. This type of gain can contribute to jitter accumulation in a chain of devices. The System 6000 gains as little as < 1dB at 2 Hz.
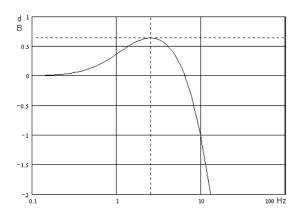
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Figure 5 Zoomed picture of the jitter rejection filter.

Lock range

There are some devices on the market that feature jitter rejection to some extent but most of them uses a common technology (VCXO type of oscillator in the PLL). This technology is limited in the terms of lock range. This means that the jitter rejection only can be done at the known frequencies e.g. 96 kHz, 88.2 kHz, 48 kHz +/- a few hundred PPM. This is typically enough given the fact that most clock oscillators have a precision of less than +/- 50ppm but if you want to use other sample rates (e.g. vary speed or the broadcast related 44.056 kHz) you will have to do without the jitter rejection.

System 6000 uses a special technology that makes it able to lock to all sample rates from: 30 to 34 kHz, 42.5 to 45.6 kHz, 46.5 to 48.5 kHz, 85 to 91 kHz and 93 to 97 kHz. This means that every signal at sample rates in these ranges will be treated with the same jitter rejection filter. The performance is not only good in a narrow range around one or two sample rates.

Intrinsic jitter

The intrinsic sampling jitter on System 6000 has been optimized through a long period of trimming in order to make the perfect AD- and DA-conversion on the ADA24/96 card. This is also why the intrinsic interface jitter is as low as < 1 ns peak, BW: 700 to 100 kHz that makes the perfect starting point for the digital setup.

System 6000 technical specifications regarding the clock circuitry:

Jitter rejection filter (4'Th order filter):	< -3dB @ 50 Hz
	< -69dB @ 500 Hz
	< -100dB @ 1.4 kHz
Jitter gain:	< 1 dB @ 2Hz
Jitter rejection at external sample rates:	30 to 34 kHz,
	42.5 to 45.6 kHz,
	46.5 to 48.5 kHz,
	85 to 91 kHz,
	93 to 97 kHz.
Internal sample rates:	96 kHz, 88.2 kHz,
	48 kHz and 44.1kHz.
Internal clock precision:	+/- 30 PPM.
Intrinsic interface jitter:	< 1 ns peak,
	BW: 700 to 100 Hz.

Measurements on System 6000

As mentioned before the higher frequency in the program signal and the higher level the more sensitive it is to jitter on the sampling clock. Therefore the measurements in this document uses a 20 kHz sine at -1 dBFS and all measurements are done at 48 kHz sample rate. The measurements are done on the DA converter on the ADA24/96 card and the test system is Audio Precision System 2 Cascade.

To show the effect of the jitter being modulated via the clock into the audio signal the measurements are FFT's of the analog signal on the ADA24/96 output.

Every full view picture is made with an FFT: 2k point, 256 times average, and equiripple window. Every frequency zoomed picture is made with an FFT: 16k point, 32 times average, and equiripple window.
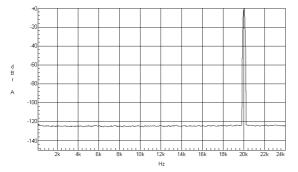
System 6000 performance

Figure 6 System 6000 DAC in master mode

The system is running in internal master mode thus there is no jitter being applied to the system. Notice the very flat noise floor with no spurious signals.
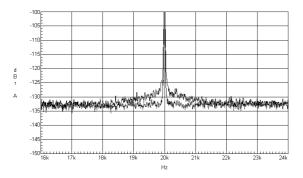

Figure 7 Zoomed version (both frq. and level) of Figure 6 plus System 6000 in slave mode.

On Figure 7 the system is running both internal master mode (lower) and external slave mode (upper) where the system is slave to the Cascade. There is no jitter being applied from the Cascade so what is shown here is approx. the difference in intrinsic jitter when the System 6000 is

slave to the digital input.
Notice that even with this much zoom the jitter on internal-mode is not visible.
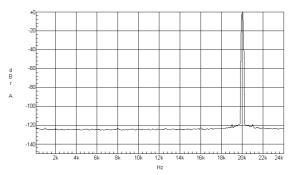The very little jitter that shows on slave-mode is low frequency weighted from 1kHz and down.

Figure 8 System 6000 DAC in slave mode, 1kHz jitter applied.

Figure 8 is a full view picture when System 6000 is slave and there is applied 1khz, 1.3us peak sine jitter. This is a huge amount of jitter and actually beyond the tolerance level specified by AES3-1992 amendment 1-1997 [3] that all AES compatible devices should be able to lock to.

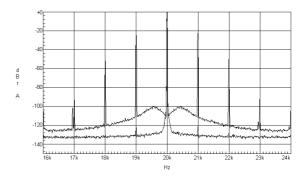**The performance of a conventional clock design compared to the performance of the System 6000**

Figure 9 Zoomed (frq. only) version of Figure 8 (lower) plus the same level of jitter applied to a conventional design (upper).

On Figure 9 the 1 kHz, 1.3 us peak sine jitter is applied to System 6000 (lower) and a conventional design (upper) without jitter rejection. Notice that the jitter spikes on the conventional design reaches -22 dB with reference to the 20 kHz tone where the System 6000 has filtered out this jitter by approx. 100 dB down to -122 dB.

There are more spikes than 20 kHz +/- 1 kHz. There are also +/- 2, 3 and 4 kHz, which are harmonics on the sine jitter generator. The low frequency noise floor on the upper curve is probably noise in the jitter generator.
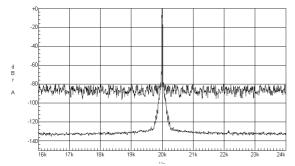
Figure 10 Zoomed (frq. only). System 6000 and conventional design in slave-mode. Wide band jitter applied.

On Figure 10 25 ns peak wide band jitter has been applied to both System 6000 (lower) and a conventional design (upper). The jitter level has formed a noise floor at approx. -80 dB with reference to the 20 kHz tone on the conventional design. The System 6000 curve reflects the jitter rejection filter curve up to approx. 300 Hz (20 kHz +/- 300 Hz on this picture). Beyond 300 Hz the System 6000 has reduced the jitter so much that it is hidden in the noise floor.

Synchronization

Synchronization: The digital signal, word clock or AES 11. There are several ways to obtain synchronization in a setup: Using a digital signal (carrying audio), a digital signal (not carrying audio) or a word clock.

• Digital signal (carrying audio).
  This is the simplest way to obtain sync and it involves only the two (or more) audio devices that are connected.

  Typically the transmitting device is the master and the receiving device is the slave.

As mentioned earlier there is jitter to take into account when selecting which device to be the master of timing. Typically the internal clock in a device is the cleanest and therefore when recording it is often the ADC that is the master (see Figure 11). To get the best DA conversion when mixing the DAC is often the master. But the DAC is a receiver of the audio signal and therefore it is necessary to send a synchronization signal from the DAC back to the rest of the system. This can be done with a digital signal that is or is not carrying audio and to which the system is slave.
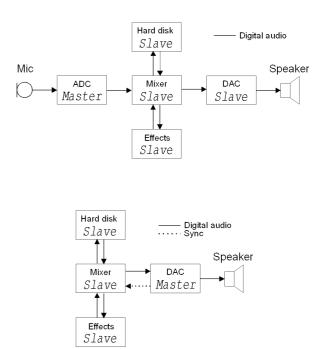

Figure 11 Digital studio setup with an ADC or DAC as master.

• Digital signal (not carrying audio) e.g. AES11 or word clock.

  This way typically involves a device that makes synchronization signals for the audio processing devices in the setup.
  This word clock generator is the master at all times and all the audio devices are slaves.

  The word clock is a square wave signal (typically TTL level, 0 to 5V) with a frequency equal to the sample rate e.g. 48kHz. The impedance is 75 ohm and the connector is RCA phono or BNC.

  The AES11 is an AES signal without audio and therefore the connector is XLR with a 110 ohm impedance.
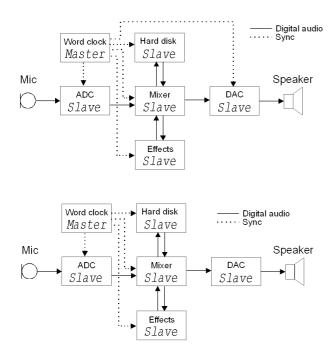
Figure 12 Same setup with a word clock generator. Example with DAC with and without word clock input.

Figure 12 shows the example setup with a word clock generator included. Some devices may not feature a word clock input and these devices will then slave to the digital signal carrying audio.

One of the advantages of using a word clock generator is that there is no constant switching between master and slave configurations. Just the normal patching signals around through the patch bay.
Another advantage is that potential jitter accumulation is reduced. The jitter sources from the clock master to where AD- or DA-conversion is done are reduced to the word clock generator intrinsic jitter, the word clock line to the converting device and the intrinsic jitter in this device. For setups with devices without word clock input the chain is a bit longer.

A disadvantage of using a setup with word clock might be that there will typically not be so much optimizing of the jitter e.g. the ADC being master when recording and the DAC being master when mixing. Even though the clock path is short (from the word clock generator to the converting device) having the converting device being the clock master could optimize the setup further jitter wise.

Nominal phase.
Digital mixers with a lot of digital inputs and other equipment e.g. surround devices have to be able to receive signals from several sources at the same time.

In Figure 13 the timing of different input and output signals is shown. AES specifies that a device must be able to

receive a signal with a phase of up to +/- 25% of the sample period away from the reference. This means that if the device is slave to input 1 the phase on the other input signals must fall within +/- 25% of the sample period away from the signal on input 1. If the phase of a signal (including two audio channels) is above the limit, the current sample in this signal can be interpreted as the previous or the next sample and this will add a delay to these specific two audio channels. A summing of the signals later in the setup (e.g. electrically or acoustically) will result in a potential audible phase error.
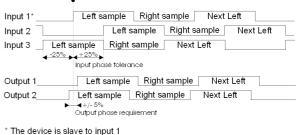

Figure 13 Nominal phase tolerances and requirements of AES signals.

It is difficult to make equipment transmitting a digital signal at exactly the same time as it receives a signal. Typically a device will have both a delay of a whole number of samples but also a sub sample delay. The delay of a whole number of samples is due to the routing of the signal in the device and the sub sample delay is due to the specific hardware in the device. AES specifies that the output must fall within +/- 5% of the sample period from the reference point (the incoming signal if the device is in slave mode). See Figure 13.
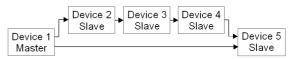

Figure 14 Example setup. Device 5 is slave to the signal from device 1.

Consider a setup like Figure 14 where device 2 to 4 adds a sub sample delay of 10% of the sample period. There will now be a difference between the two signals going into device 5 of 30% of a sample period. Now device 5 might interpret the two inputs wrong the way mentioned above. In a whole number of samples this might not be a problem because device 2 to 4 also has perhaps 10 samples delay pr. device equals a total delay of 30. So the resulting 1 sample extra delay in this chain due to several sub sample delays might not matter.

Another problem might be that perhaps the jitter level after device 4 is quite high. This jitter will perhaps make the signal from device 4 continuously cross the point in device 5 where the signal is interpreted as the current sample or

the next. This will make continuous slip samples (perhaps with audible clicks) on the input on device 5 receiving signal from device 4.

A way to work around this could be to have device 3 slaving directly to device 1 with an extra synchronization signal. This way the 10% sub sample delay in device 2 will be eliminated. A setup using word clock generator will typically not suffer from this kind of problem due to every device being slave to the same reference. Therefore there will not be any chain of devices that potentially could accumulate phase errors.

ADAT interfaces are typically more sensitive to sub sample delays or phase offsets than AES interfaces.

System 6000 technical specifications regarding in and output phase:

Digital Output Phase: < 3 % of sample period
Input Variation Before
Sample Slip: +27 % / -73 % of sample period

Literature:
[1] Jitter: Specification and Assessment in Digital Audio Equipment by Julian Dunn.
Presented at AES 93rd Convention, October 1992
Available at www.nanophon.com

[2] Audio Precision, Technotes by Julian Dunn.Technote 23, 24 and 25.
Available at www.ap.com

[3] Standard: AES3-1992 amendment 1-1997.
Available at www.aes.org

Other literature on the subject:
"Everything you always wanted to know about jitter but where afraid to ask" by Bob Katz.
Available at www.digido.com

Measurement systems manufactured by:
Audio Precision www.ap.com
Prism Sound www.prismsound.com